Improved Delta Sigma Modulators for High Speed Applications

David Gautier, Michel Robbe, Stephan Doucet, Renaud Lemoine, Smail Bachir, Claude Duvanaud

Improved Delta Sigma Modulators for High Speed Applications

David Gautier[1,2], Michel Robbe[1], Stephan Doucet[1], Renaud Lemoine[1]
Smail Bachir[2] and Claude Duvanaud[2]
[1] ACCO SEMICONDUCTOR, 36-38 rue de la princesse, 78430 Louveciennes , France
[2]LAII-EA 1219, Universite de Poitiers, IUT -4 avenue de Varsovie, 16021 Angouleme
Email[1]: david.gautier, michel.robbe, stephan.doucet, renaud.lemoine@acco-semi.com
Email[2]: claude.duvanaud, smail.bachir@univ-poitiers.fr

***Abstract*—This article presents a new LowPass Delta Sigma Modulators (LPDS) architecture to improve the noise shaping for high frequency applications. The errors resulting from approximations made by calculating with $1/2^N$ coefficients are compensated. Simulations with extracted parasitics of the layout are made and give a SNDR of 111dB, 3.8mW power consumption at 4GHz in 65nm CMOS technology for UMTS standard.**

I. Introduction

The world of mobile telecommunications is in constant evolution. The appearance of new services leads to increases in bandwidth and carrier frequencies. Furthermore, the power consumption of mobile devices must be as low as possible in order to increase the usage time of batteries.

These constraints suggest the use of circuit blocks with high efficiency at high frequencies. A "full-digital" system would achieve these goals more easily than a RF analog system because digital technology has many advantages. First, use of digital CMOS technology allows for a reduction in cost, die area and energy consumption. Second, a nano-scale technology allows for operation at high sampling frequencies. Finally, a digital system is easily reconfigurable in order to have a multi-standard chip.

The "full-digital" system described herein is composed of two parts. The first part is configured to shape the signal from the base band using interpolators and Delta Sigma Modulators (DSM) like [1]. The second part amplifies the signal prior to transmission. For the second part, a high efficiency switching mode power amplifier (PA) is used. The approach of using these different parts in an emitter was first presented by A. Jayaraman and al. [2] .

This article focuses primarily on a LPDS modulator. Improvements were made over a classical feedback modulator of the *Cascade-of-Integrators FeedBack* (CIFB) type [3]. This modulator has been optimized in order to compensate the errors resulting from approximations made by calculating with $1/2^N$ coefficients. By re-injecting this error in the loop through an appropriate structure, it is possible to improve the noise shaping. In section II, a comparative study between a classical LPDS and the proposed LPDS is discussed. Section III, describes the implementation of the LPDS in 65nm CMOS technology and presents layout extraction (Resistors + Capacitors + Coupling Capacitors, (R+C+CC)) simulation results in term of Signal to Noise and Distortion Ratio (SNDR) and coding efficiency (η).

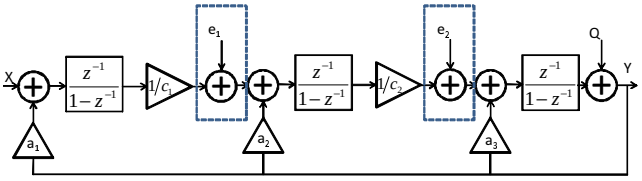


Fig. 1. Classical third order LPDS with added noise sources to represent truncation errors

II. Comparison between a classical LPDS and the new LPDS

A. Classical LPDS

Fig.1 presents a typical LPDS architecture used in digital modulators. All coefficients are represented by power of two in order to simplify the calculations. To minimize the number of bits in the LPDS, $1/c_i$ coefficients are used after the integrator. However in a digital LPDS, calculations are made with integer numbers so the use of coefficients like $1/2^N$ leads to introduction of truncation errors. In pratice the N Least Significant Bits (LSB), which represent the truncation error, are lost.

A LPDS can be described by two transfer functions, a Signal Transfer Function (STF) and a Noise Transfer Function (NTF). The truncation error can be represented by noise sources e_i added after the coefficients as illustrated in Fig.1. With these two noise sources, a new NTF can be calculated (X = 0) :

$$\begin{array}{l} Y = \Omega(z).(Q + D1(z).e_1 + D2(z).e_2) \\ \frac{Y}{Q} = NTF_{ideal} = \Omega \\ \frac{Y}{e_1} = NTF_{e_1} = \Omega(z).D_1(z), \frac{Y}{e_2} = NTF_{e_2} = \Omega(z).D_2(z) \end{array} \quad (1)$$

$$\Omega(z) = \frac{(1-z^{-1})^3}{1 + d_1.z^{-1} + d_2.z^{-2} + d_3.z^{-3}}$$

where $D1(z) = \frac{z^{-2}}{c_2.(1-z^{-1})^2}$ and $D2(z) = \frac{z^{-1}}{(1-z^{-1})}$ We

$$\begin{array}{l} d_1 = a_3 - 3 \ ; \ d_2 = 3 + a_2/c_2 - 2.a_3 \\ d_3 = a_3 - 1 - a_1 - a_2/c_2 \end{array}$$

make the approximation that the quantification error Q and

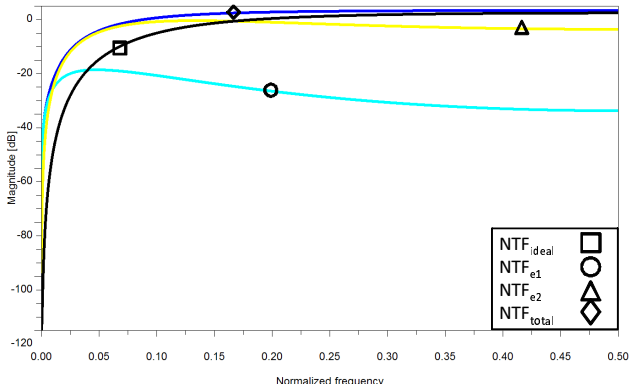


Fig. 2. NTF without correction

the truncation errors e_1 and e_2 are white noise sources with the same variance (σ). So, it is possible to determine the total NTF (NTF_{total}) which represents the global noise shaping of the LPDS.

Fig.2 displays the three NTF $(NTF_{ideal}, NTF_{e_1}, NTF_{e_2})$ and their sum (NTF_{total}). As can be seen, the noise source e_1 increases the noise in the normalized frequency band [0 ; 0.04] and the noise source e_2 increases the noise in the normalized frequency band [0 ; 0.17] compared with the NTF_{ideal}. So the truncation errors increase the noise in the lower frequencies and as a result decrease the SNDR.

B. Improved LPDS

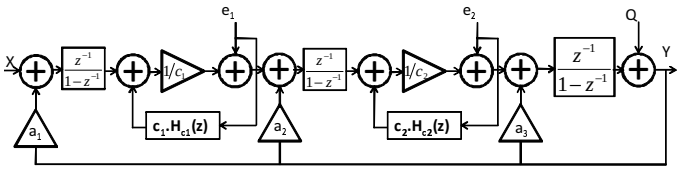
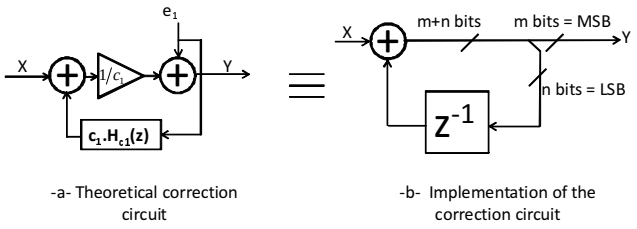


Fig. 3. Third order LPDS with truncation error correction

As discussed above, the truncation errors due to the calculations, with $1/2^N$ coefficients, decrease the SNDR because the two new noise sources are added (e_1 and e_2). In order to decrease the impact of these two noise sources, the truncation error (deleted bits) are re-injected before the coefficients through a filter as shown in Fig.3. In two's-complement arithmetic, a division of an integer ($[0; 2^k - 1]$) with a $1/2^N$ coefficient consists in separating the m Most Significant Bits (MSB) where $m = k - N$ and n LSB where $n = N$. The sign of the integer is kept by the *m* MSB and the *n* LSB are always positive within range of $[0; 2^n - 1]$.

The filters H_{c_i} are not necessarily the same and each can be designed in order to compensate for the NTF_{e_1} and NTF_{e_2}, respectively. We now consider the correction circuits $H_{c_1} = H_{c_2} = z^{-1}$, illustrated in Fig.4. The equations (2) give the news values of D_1 and D_2 with the correction circuits :



-a- Theoretical correction circuit

-b- Implementation of the correction circuit

Fig. 4. Representation of theoretical and implemented correction circuits

$$\begin{cases} \Omega = \dfrac{(1-z^{-1})^3}{1 + d_1.z^{-1} + d_2.z^{-2} + d_3.z^{-3}} \\ D1 = \dfrac{z^{-2}}{c_2.(1-z^{-1})} \text{ and } D2 = z^{-1} \end{cases} \quad (2)$$

As shown by these equations, the ideal NTF (Ω) is not modified. The correction circuits change only the noise shaping of the truncation errors. Source e_1 is integrated and delayed once, and e_2 is delayed of one step. Fig.5 shown the new NTF. Source e_1 increases the noise in the band [0 ; 0.01] and e_2 leads to the same noise shaping as the quantization error Q. The noise due to the truncation errors is reduced so the NTF_{total} is closed to the NTF_{ideal} relative to the NTF_{total} of the uncorrected LPDS, compared with Fig.2.

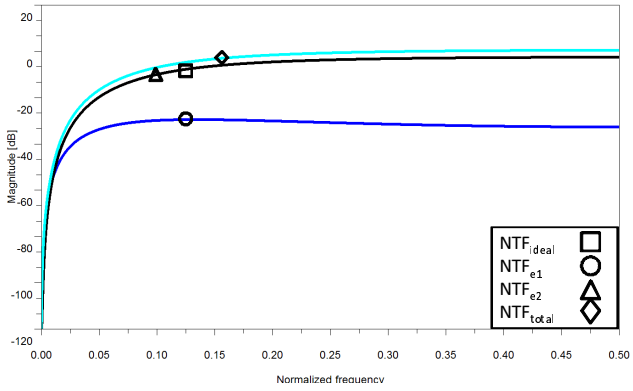


Fig. 5. NTF with correction circuit

C. Comparison of the two LPDS

We have demonstrated that it is possible to improve the noise shaping of a LPDS by taking into account and correcting the truncation error. In order to verify this improvement a simulation is made with a 2.5MHz sinusoidal input and a sampling frequency of 3.96GHz. Fig.6 shows the output spectrum of the two LPDS. In the twenty first MHz, the noise is reduce by 25dB with the improved LPDS. The noise shaping is also better in the [0;200]MHz band with the proposed LPDS relative to the classical LPDS. Potentially, using two improved LPDS in an IQ transmitter as described in [4] [5] would allow a noise decrease in a band of $400MHz$ centered on the carrier frequency. We break down the LPDS in three stages. The first and second stages are composed of an integrator and a correction circuit (or a $1/2^N$ coefficient for the classical

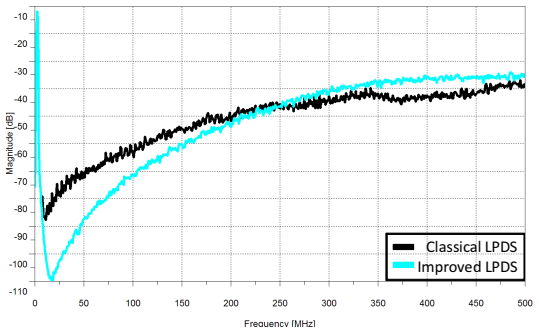


Fig. 6. Comparison between the output spectrum of the 2 LPDS for a 2.5MHz sinusoidal input at 3.96GHz sampling frequency

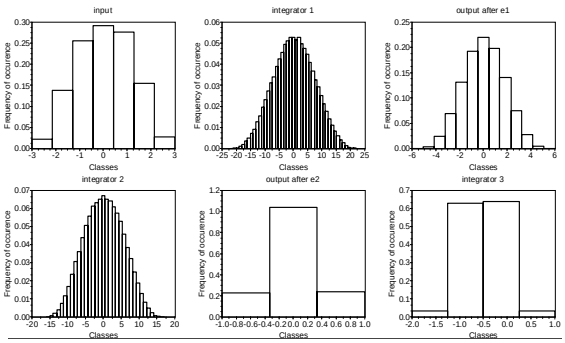


Fig. 8. Histograms of each signal in the three stages for a WCDMA signal input

LPDS). The third stage includes the last integrator. Observing the signal after the integrators and the correction circuits (or $1/2^N$ coefficient), one can see why the noise increases in the low frequencies in a classical LPDS. Fig.7 represents the histograms of each signal for the different LPDS. In the first stage, signals have the same dispersal. Nevertheless, after the integrator of the second stage, a non-zero offset appears in the classical LPDS case. This offset is due to the integration of the truncation error which leads to an increase in the noise at low frequency. Reduction of the truncation error using the correction circuit discussed herein decreases this offset close to zero and as a result reduces the noise at low frequency. Operation with the $1/c_2$ coefficient reduces considerably the number of bits, and the representation of signals is centered around zero. In the third stage, the truncation error results in further offset at the integrator output. This offset is again reduced when the correction circuit is included in the DSM. The correction circuit results in an output of the integrator that is approximately symmetric around zero. As can be seen in

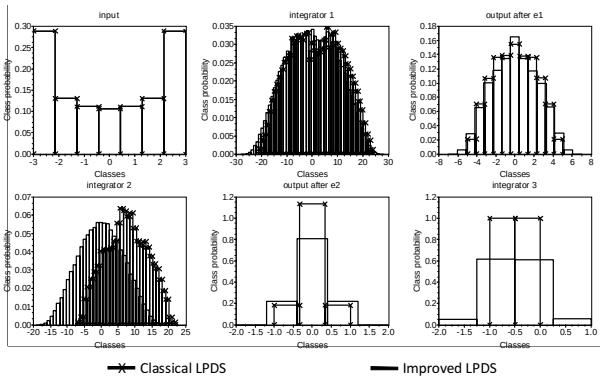


Fig. 7. Histograms of each signals in the three stages for the two LPDS

Fig.7, the correction does not change the variance (σ^2) of each signal as compared to the classical LPDS. There is the same number of useful bits in each of the two LPDS.

III. Implementation of the corrected LPDS

A. Number of useful bits

The main design objectives are the total power consumption, the die area and the maximum sampling frequency (F_s). The use of a correction circuit does not increase the number of useful bits in the LPDS as can be seen in II-C. Fig.8 represents the simulated histograms of signals within the improved LPDS with a WCDMA input signal. The 12 bits WCDMA input signal sampled at 3.84MHz has been interpolated to F_s and shape once by a multi-bit Multi-stAge noise SHaping (MASH)[6] LPDS in order to have 4 bits at the third order LPDS input. These histograms illustrate the number of useful bits with this type of input. As can be seen, the two first integrators have the maximum dispersal, $[-22; 22]$ and $[-16; 17]$ respectively. Number of useful bits is the number of bits required to represent this dispersal and a sign bit. In this LPDS and for this input signal, the number of useful bits is 6 (5 bits for the number and 1 for the sign).

B. First and second stage topology

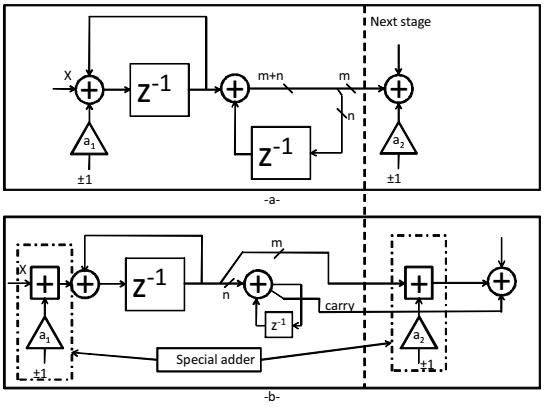


Fig. 9. -a- First stage topology -b- First stage optimized in order to have adder with only 2 inputs

Fig.9-a displays the schematic of the first stage (which may be the same in the second stage). This stage is defined in two parts. A first part includes an adder with three inputs and a

delay cell (i.e. D-latch) which consists in an integrator and feedback. A second part includes a D-latch and an adder with two inputs, which form the correction circuit. The adder of the correction circuit is in series with the first adder of the second stage. These two adders are equivalent to an adder with four inputs. In order to have the maximum sampling frequency, adders should have a minimum number of inputs and each input should have the minimum number of bits. The minimum number of input is two (without the carry input). One can modify the schematic of Fig.9-a to optimize the number of inputs for each adders. Fig.9-b shows an example of this optimization. In this new schematic, two "special adders" are used. They are configured, with judicious choice of the a_i coefficients, to inverse the sign bit of the first input as shown in Fig.10.

Fig. 10. Special adder for the optimized LPDS

C. R+C+CC simulation results

The improved LPDS discussed herein has been implemented in 65nm CMOS technology. All cells (NOR, NAND, etc) are designed in classical static logic, excepted XOR and XNOR which used Passgate logic. Simulations are made from layout parasitics extraction R+C+CC. Table I gives the main characteristics of the LPDS. Two simulations are made, with

TABLE I
LPDS MAIN CHARACTERISTICS

Specifications	Values
Max F_s	4GHz
Power consumption	3.8mW
Area	140μm x 20μm

and without correction circuit, in order to estimate the SNDR and the coding efficiency. They are evaluated for a GSM and UMTS cases.

Coding efficiency is a criteria to evaluate the efficiency of the encoding method. LPDS generates a pulse train with an amplitude levels of $\pm\Delta_p$ and a total power is Δ_p^2. P_s is the power of the output signal as defined in the following equation.

$$P_s = \int_0^{f_b} S_p(f)df \tag{3}$$

where $S_p(f)$ and f_b are respectively the power spectral density of the pulse train and the bandwidth. The coding efficiency of the LPDS is then :

$$\eta = \frac{P_s}{\Delta_p^2} \tag{4}$$

For GSM, SNDR is calculated by integrating the noise over a bandwidth of 100kHz and for UMTS over a bandwidth of 2.5MHz. Furthermore, SNDR is calculated as a function of the output signal power in order to be independent of the STF gain. For both standards, sampling rate is set to 4Ghz.

Fig.11 shows the SNDR and the coding efficiency versus the input amplitude for the different standards. For UMTS a peak SNDR of 80.9dB and 111dB is achieved and the corresponding coding efficiency is 1.5% and 4.84% respectively without and with corrector. For GSM a peak SNDR of 126dB and 181dB is achieved and the corresponding coding efficiency is 1.53% and 4.83% respectively without and with corrector.

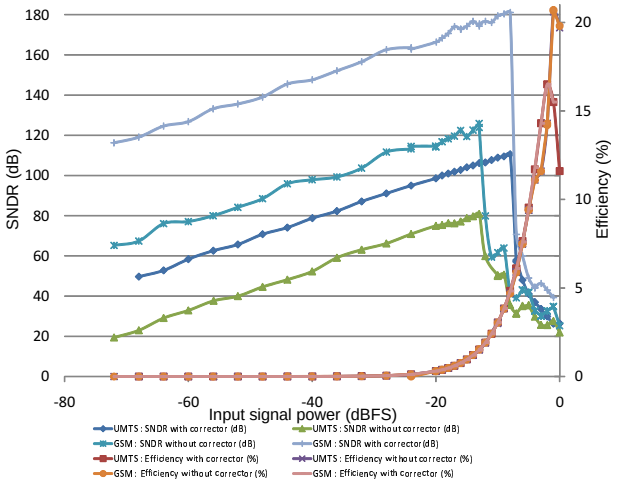


Fig. 11. SNDR and Coding efficiency with and without corrector

IV. Conclusion

A new architecture of LPDS is proposed in this paper. This new architecture is based on the re-injection of the truncation error in order to increase the SNDR and the coding efficiency. Compared with a classical LPDS, SNDR is improved of 30dB, η is three time better and only 6 bits are used. The simulations with extracted parasitics shows a power consumption of 3.8mW@4GHz. More complex correction circuit with higher order LPDS can be used to improve the noise shaping even more.

References

[1] A. Jerng and C.G. Sodin, A Wideband $\Delta\Sigma$ Digital-RF Modulator for High Data Rate Transmitters IEEE JOURNAL OF SSC, vol.42, n8, 2007.

[2] Jayaraman A.; Chen P.F.; Hanington G.; Larson L.; Asbeck P., Linear high-efficiency microwave power amplifiers using BPDSM , IEEE microwave and guide wave letters, vol 8, n3, pp. 121-123, Mar 1998.

[3] R. Schreier and Gabor C. Temes, "Understanding delta sigma data converters" *book published by John Wiley & Sons Inc.*, 2005.

[4] A. Frappe, B. Stefanelli, A. Flament, A. Kaiser and A. Cathelin, "A digital Delta Sigma RF signal generator for mobile communication transmitters in 90nm CMOS" *IEEE RFIC symposium*, pp. 13-16, June 2008.

[5] M. Helaouil, N. Demirel2, R. NegraI, S. BoumizaI, E. Kerherve2, A. Ghazel3, F.M. Ghannouchil, "Digitally Optimized DSM for WiMAX Transmitter Design" *IEEE Radio and wireless symposium*, pp. 419-422, Jan 2007.

[6] L. A. Willams, III and B. A. Wooley, "Third-order cascaded sigma delta modulators" *IEEE Trans. Ciruits Sys*, vol. CAS-38, pp. 489-498, May 1991.